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Silicon Interfacial Passivation Layer Chemistry for High-*k*/InP Interfaces

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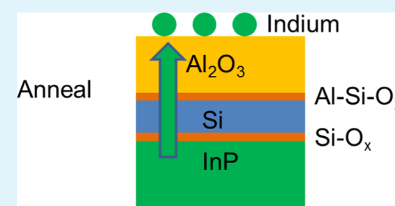
ABSTRACT: The interfacial chemistry of thin (1 nm) silicon (Si) interfacial passivation layers (IPLs) deposited on acid-etched and native oxide InP(100) samples prior to atomic layer deposition (ALD) is investigated. The phosphorus oxides are scavenged completely from the acid-etched samples but not completely from the native oxide samples. Aluminum silicate and hafnium silicate are possibly generated upon ALD and following annealing. The thermal stability of a high-*k*/Si/InP (acid-etched) stack are also studied by in situ annealing to 400 and 500 °C under ultrahigh vacuum, and the aluminum oxide/Si/InP stack is the most thermally stable. An indium out-diffusion to the sample surface is observed through the Si IPL and the high-*k* dielectric, which may form volatile species and evaporate from the sample surface.



KEYWORDS: *silicon interfacial passivation layer, indium phosphide, high-k, diffusion, atomic layer deposition*

■ INTRODUCTION

Group III−V metal oxide semiconductor field-effect transistors (MOSFETs) are strong contenders to replace silicon (Si) in future generations of high-mobility transistor devices.[1,2] InP is a potential candidate for use as a barrier layer for such devices.[3,4] The addition of this barrier layer moves the channel materials away from the high-*k* dielectric, with the aim being to minimize the defects generated by oxidation of the channel materials.[5] However, the interfacial quality between InP and the high-*k* dielectrics still affects the electrical performance of the devices, having an impact on the electrical performance, such as the subthreshold swing.[6] Therefore, engineering this InP/high-*k* interface is urgent to obtain an optimized electrical performance. The incorporation of a thin aluminum silicate (Al-silicate) layer between an InP barrier layer and high-*k* dielectric has been proposed.[7] However, no experimental results are reported. Generally, there are two strategies to grow this Al-silicate overlayer: one way is through a codeposition process, while another method is through deposition of a thin layer of Si onto InP, followed by Al_2O_3 growth and/or upon further annealing. The Si/InP interface study also benefits the solar cell research community because of correlation of the surface quality with the surface recombination velocity.[8]

On the basis of previous in situ atomic layer deposition (ALD) of high-*k* oxides half-cycle reactions on InP/GaP using X-ray photoelectron spectroscopy (XPS) for acid-etched and native oxide surfaces, the concentrations of phosphorus oxides (P-oxides) remains significant after exposure to the first pulse of the metal precursor and following initial reaction stages.[9−11] S-Passivation by $(NH_4)_2S$ can significantly decrease the P-oxide concentration, but the P-oxide peaks remain slightly above the XPS detection limit after 10 cycles of the ALD process. Also, a previous study looking at the impact of postdeposition annealing on the electrical performance of these structures indicated that an increase in P-rich oxides is correlated to an increase in the interface state densities (D_{it}).[12] Therefore, it is critical to control the concentration of indium (In)−P-oxides prior to high-*k* dielectric growth.

Recently, several reports have demonstrated that In out-diffusion can take place through the high-*k* dielectric from both native oxide and S-passivated InP samples upon the ALD process and postdeposition annealing.[13−15] The resulting P-rich oxides at the InP/high-*k* interface have also been hypothesized to be correlated to D_{it}.[14] This elemental diffusion further highlights the importance of alternative InP surface passivation prior to ALD.

In this work, a thin (1 nm) interfacial passivation layer (IPL) of amorphous Si is deposited by plasma-enhanced chemical vapor deposition (PECVD) with the aim of scavenging In and P-oxide states from the interface, prior to high-*k* ALD and preventing oxide regrowth[16] during high-*k* oxide deposition. Using in situ XPS to prevent atmospheric exposure after high-*k* dielectric deposition, we investigated the interfacial chemistry of the high-*k*/Si/InP stack and the thermal stability of the interfaces following in situ annealing up to 400 and 500 °C under ultrahigh vacuum (UHV). Ex situ low-energy ion scattering spectroscopy (LEIS) was also used to characterize the first atomic layer chemical compensation after UHV annealing at 500 °C.

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EXPERIMENTAL METHODS

Four n-type InP (100) samples purchased from AXT and cleaved from the same wafer were used in this study. All samples were degreased by dipping in acetone, methanol, and isopropyl alcohol for 1 min each at room temperature (RT) before further specific processing (see Table 1). Sample A was deposited with 1 nm of amorphous Si immediately after degreasing and transferred into the UHV system within 10 min. Sample B was deposited with 1 nm of Si after degreasing, followed by a two-step piranha/HCl etching of short duration (<5 min),[17] and then exposed to 20 cycles of Al_2O_3 ALD, resulting in a photoelectron transparent layer to the substrate. The process of the two-step piranha/HCl etch entailed dipping of the InP wafer into H_2SO_4:H_2O_2:H_2O = 4:1:100 for 2 min followed by HCl:H_2O = 1:3 for 2 min, where the initial concentrations of H_2SO_4, H_2O_2, and HCl were 96%, 30%, and 36%, respectively.[18] The samples were rinsed with deionized (DI) water after acid treatment. Sample C was deposited with 1 nm of Si after degreasing and the two-step acid etch and then underwent 20 cycles of HfO_2 ALD. Samples A–C were all annealed to 400 and 500 °C under UHV (base pressure ~10^{-10} mbar). Sample D was degreased and treated with the two-step acid etch, and sample E was degreased only. Both samples D and E are used as the InP surface control samples in this work.

Table 1. Process for Each Sample Studied (× Indicates Process Not Applied)

sample A	degrease	×	Si IPL	Al_2O_3	400 °C	500 °C
sample B	degrease	acid etch	Si IPL	Al_2O_3	400 °C	500 °C
sample C	degrease	acid etch	Si IPL	HfO_2	400 °C	500 °C
sample D	degrease	acid etch	×	×	×	×
sample E	degrease	×	×	×	×	×

Si PECVD was carried out ex situ in a Plasma-Therm model 790 PECVD system (capacitively coupled 13.56 MHz source), with a SiH_4 flow rate of 100 SCCM and a helium gas flow of 400 SCCM at 200 °C.

The UHV system used in this study is capable of various in situ deposition methods and has characterization tools for standard UHV analysis, described elsewhere.[19] An analysis chamber, with monochromatic XPS ($h\nu$ = 1486.7 eV) used to characterize the interfacial chemistry, is connected to a Picosun ALD reactor and the physical vapor deposition chamber using a UHV transfer tube (~10^{-10} mbar). This setup enables samples to be transferred between deposition and analysis chambers without exposure to air. The XPS system is equipped with a seven-channel hemispherical detector, and all XPS spectra are taken at 45° with respect to the sample surface with a pass energy of 15 eV. Spectral deconvolution was accomplished using the peak-fitting software *AAnalyzer*.[20]

LEIS is used in this study to determine the identity of the atoms present exclusively on the sample surface.[21] The LEIS scans were taken using a Qtac[100] IonTOF detector, which enables extremely high efficiency in detecting the scattered ions so that a low dose of ions can be used during the scan, minimizing modification of the sample surface due to incident noble gas ions. He^+ (3 keV) and Ne^+ (5 keV) were used on the Al_2O_3/Si/InP and HfO_2/Si/InP stacks, respectively. The He^+ ions provide higher-energy resolution for low mass elements (i.e., Al, O, P), and the Ne^+ ions provide higher-energy resolution for higher mass elements (i.e., Hf, In).

Al_2O_3 and HfO_2 ALDs were both conducted by a sequence of metal precursor/purge/oxidant precursor/purge of duration 0.1 s/20 s/0.1 s/20 s. Trimethyaluminum (TMA) was used as the Al metal precursor, and DI water vapor was used for the oxidant precursor for ALD Al_2O_3. The TMA and DI water vessels as well as the delivery lines and valves were maintained at RT during deposition. Tetrakis(dimethylamido) hafnium was used as the hafnium (Hf) metal precursor for HfO_2 deposition, was maintained at 90 °C, and delivered through heated lines/valves (135 °C) into the ALD reactor. DI water vapor was also used as the oxidant for HfO_2 deposition. Al_2O_3 and HfO_2 ALDs were conducted at a substrate temperature of 300 and 250 °C, respectively. To account for band bending and charging effects in the XPS, spectra, the P 2p peak is set at a binding energy (BE) of 128.9 eV.[9]

RESULTS AND DISCUSSION

Figure 1a shows the P $2p_{3/2}$ spectra from sample A after the process steps shown in Table 1, including Al_2O_3 ALD (the thickness of 1.4 nm is calculated based on attenuation of the P 2p spectra) and subsequent UHV annealing at 400 and 500 °C. The thickness of Al_2O_3 on this Si/InP stack is thinner than that obtained on the InP native oxide control sample, where 2 nm of Al_2O_3 is deposited under the same ALD conditions. This thinner Al_2O_3 film is speculated to correlate with H-termination of the Si surface during the PECVD process,[22,23] which requires the initial incubation cycles to grow uniformly for the short precursor exposure time employed in this study.[24,25] The peak with a BE at 128.9 eV is assigned to the InP bulk bonding, and the peak with higher BE (labeled "P–O" in Figure 1a) is assigned to the formation of P-oxides.[26] A decrease in the concentration of P-oxides is seen after Si deposition, and the P-oxide concentration remains nearly constant throughout the subsequent process steps.

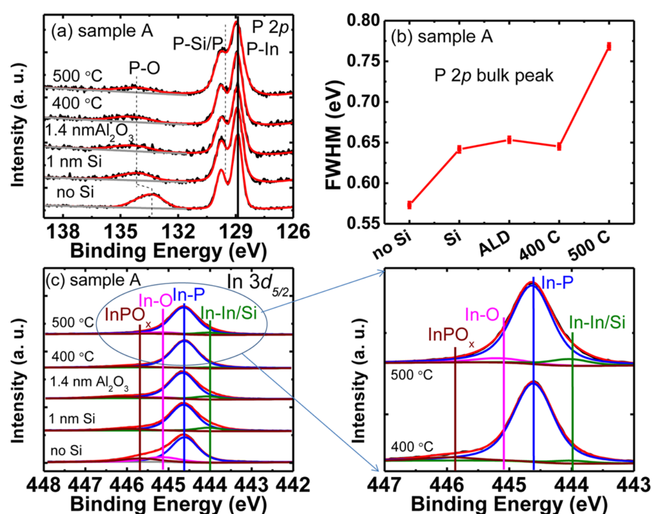

Figure 1. XPS from sample A before Si deposition, after Si deposition, after Al_2O_3 ALD, and after annealing at 400 and 500 °C under UHV; (a) P 2p; (b) FWHM of the P 2p bulk spectra; (c) In $3d_{5/2}$ with outset showing the spectra after UHV annealing.

Figure 1b shows the full width at half-maximum (FWHM) of the InP bulk peak. An increase in the FWHM is seen after Si deposition, suggesting the development of an alternative chemical state and possibly P–Si and/or P–P ("P–Si/P") bond formation during the PECVD process. (The limited energy resolution prohibits deconvolution of the P–Si and P–P chemical states detected here.)

Figure 1c shows the In $3d_{5/2}$ spectra of sample A again at each stage of the five-step process. The peak with a BE separation of +0.54 eV to the InP bulk peak (at 444.6 eV) is assigned to In–oxygen (O) bonding,[11] and the peak with a BE separation of +1.1 eV to the InP bulk peak is assigned to $InPO_x$ [possibly $InPO_4$/$In(PO_3)_3$].[27] The total oxide concentration is seen to decrease significantly after Si deposition and is concomitant with the detection of In–In and/or In–Si ("In–In/Si") bond formation emerging from the spectra background. (The limited energy resolution prohibits deconvolution of the In–In and In–Si chemical states detected here.) No detectable

change is observed after the Al_2O_3 ALD step, and a significant decrease in the In-oxide and In–In/Si concentration is observed after the 400 °C annealing. However, after annealing at 500 °C, an increase in the concentration for both In–In/Si and In-oxides is detected. Therefore, for sample A, annealing at 400 °C results in minimal interfacial oxide formation.

Figure 2 shows the Si 2p and Al 2p spectra of sample A after the process steps as well. For the Si 2p spectra (Figure 2a), the

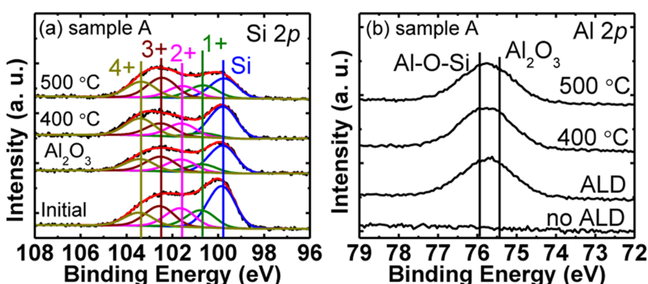

Figure 2. XPS core level spectra from sample A: (a) Si 2p and (b) Al 2p upon Si deposition, after Al_2O_3 ALD, and after annealing at 400 and 500 °C under UHV.

peaks with BE separations of +0.9, +1.8, +2.7, and +3.6 eV relative to the Si–Si peak (at 99.6 eV) are assigned to Si-suboxide 1+, 2+, and 3+ and SiO_2 4+ states, respectively.[28] The Si 1+ state is seen to convert to higher oxidation states upon Al_2O_3 ALD and is below the XPS detection limit after annealing at 400 °C under UHV. The Si–Si bond concentration is seen to decrease significantly after annealing at 500 °C, concurrent with an increase of the Si-suboxides.

The Al 2p spectra (Figure 2b) indicate possible Al-silicate formation upon ALD and further annealing. It is difficult to quantitatively analyze the contributions of Al-silicate and Al_2O_3[29] because the energy separation between these two states is only ~0.4 eV[30] and the Al-oxide peaks are relatively wide (FWHM ~ 1.5 eV for Al $2p_{3/2}$). The increase of the Si total peak area and the decrease of the Al total peak area are consistent with an intermixing of Si and Al, suggesting Al-silicate formation upon annealing at 400 and 500 °C. Thus, the final stack upon annealing is likely Al-silicate/Si/$InPO_x$/InP. Al-silicate formation is thermodynamically favorable, according to the Al–Si–O phase diagram at these annealing temperatures.[31]

Figure 3 shows the P 2p and In $3d_{5/2}$ spectra from sample B. P-oxides are seen to be scavenged below the XPS detection limit upon Si deposition, and no significant change is seen upon further processing. Figure 3b shows the FWHM of the bulk peak of P 2p at different process steps. An increase in the FWHM of the P 2p peak is seen upon Si deposition, indicating P–P/Si bond formation during the Si PECVD process. The FWHM is seen to decrease after Al_2O_3 ALD and UHV annealing, suggesting that the bonding environment has decreased, possibly related to decreases in the P–P/Si concentration.

As seen in Figure 3b, the In–O concentration is also observed to decrease below the XPS detection limit upon Si deposition, and an In–In/Si feature again emerges from the spectral background. This In–In/Si bond concentration is seen to decrease upon Al_2O_3 deposition and annealing at 400 °C and is close to the XPS detection limit after annealing at 500 °C. It is noted that In–In and P–P have been correlated to states within the InP energy band gap and could degrade the device performance.[32] Therefore, annealing at 500 °C is seen as

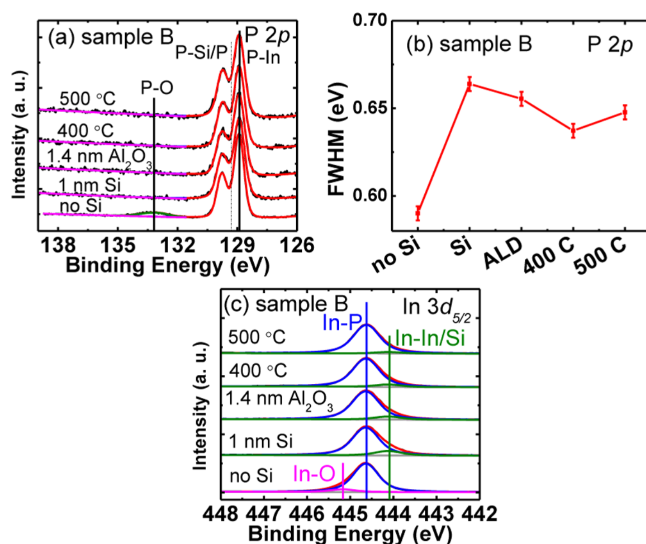

Figure 3. XPS from sample B before Si deposition, after Si deposition, after Al_2O_3 ALD, and after annealing at 400 and 500 °C under UHV: (a) P 2p; (b) FWHM of the P 2p bulk spectra; (c) In $3d_{5/2}$.

optimum in this study, in terms of minimizing In–In/Si and P–P bond formation.

In–P-oxide formed on the InP surface after acid etching is only a monolayer thick according to the XPS intensity. Therefore, the Si PECVD readily reacts with the thin surface oxide layer. In contrast, the native oxide associated with InP (samples D and E, not shown) is somewhat thicker 2 nm). It has been shown previously that In out-diffuses through even thicker (5.6 nm) oxide films upon comparable thermal treatments, but P out-diffusion is relatively inhibited.[14] Moreover, upon complete Si reaction with the surface P-oxide, further scavenging through Si–O formation is likely also inhibited. This proposed mechanism may explain why Si can scavenge P-oxides completely from the acid-etched sample but not from the thicker native oxide sample. In addition, the H radicals generated during the PECVD process (coming from the SiH_4 and helium plasma) may also be hypothesized to contribute to the decrease of In–P-oxide concentration, which is similar to the cleaning effect of the native oxide on the InP surface by atomic H.[33]

Figure 4 shows the Si 2p and Al 2p spectra for sample B. A decrease in the Si 1+ state concentration is detected, concurrent with an increase in the concentration of higher oxidation states (3+ and 4+). The higher oxidation Si states are possibly related to Al-silicate formation.[34] From the Al 2p spectral line shape, a possible Al-silicate species is formed after ALD and following

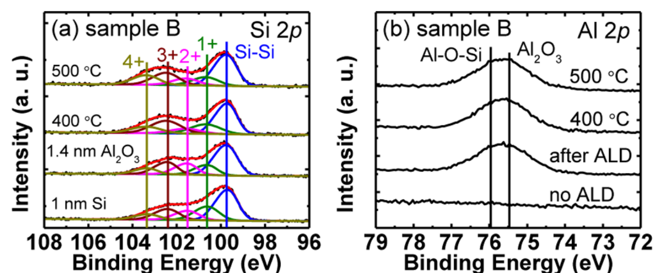

Figure 4. XPS from sample B, upon Si deposition, after Al_2O_3 ALD, and after annealing at 400 and 500° under UHV: (a) Si 2p; (b) Al 2p.

UHV annealing (Figure 4b). Again, it is difficult to quantitatively deconvolute the Al 2p spectra, but silicate formation is consistent with prior reports on Si substrates.

Figure 5 shows the P 2p and In $3d_{5/2}$ spectra from sample C. (A HfO_2 thickness of 1.3 nm is estimated from the P 2p attenuation.) From the P 2p spectra, the deposited Si has again scavenged the P-oxides completely, and the InP bulk peak is not seen to change significantly upon HfO_2 ALD and 400 °C annealing. However, the P 2p bulk spectra appear to have broadened significantly after annealing at 500 °C. This broadening is also evidenced from the FWHM of the P 2p bulk peak (Figure 5b).

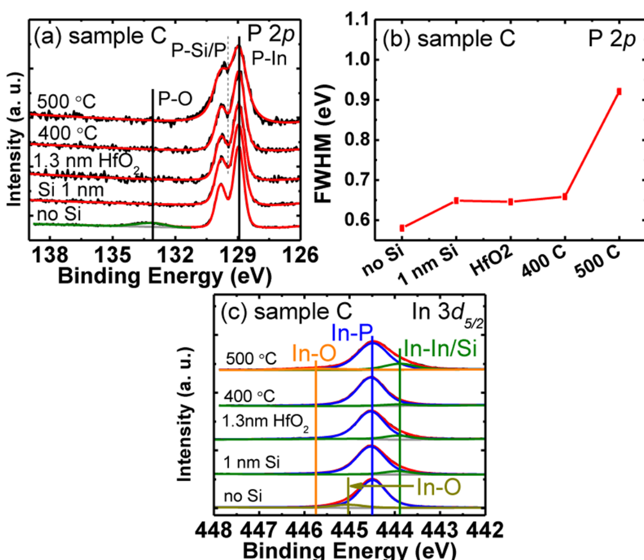

Figure 5. XPS from sample C before Si deposition, after Si deposition, after HfO_2 ALD, and after annealing at 400 and 500 °C under UHV: (a) P 2p; (b) FWHM of the P 2p bulk spectra; (c) In $3d_{5/2}$.

From the In $3d_{5/2}$ spectra (Figure 5c), Si deposition has similarly scavenged the In-oxides (expected in the 445 to 446 eV range)[34] below the XPS detection limit and also resulting in In−In/Si bond formation. The In-oxide concentrations are below the XPS detection limit upon HfO_2 deposition and the first annealing at 400 °C, but In-oxides are subsequently detected after the second annealing at 500 °C. In contrast, the In−In/Si bond concentration is not seen to change significantly upon HfO_2 ALD, but this feature intensity is close to the detection limit of XPS after the 400 °C annealing and seen to increase after the 500 °C annealing. Therefore, the ideal annealing temperature for the HfO_2/Si/InP stack is 400 °C, in terms of minimizing the formation of P- and In-oxides as well as the In−In/Si bonds.

Figure 6 shows the Hf 4d and Si 2p spectra for sample C. Peak broadening upon annealing is detected from the FWHM of the Hf 4d spectra (Figure 6b), suggesting possible Hf-silicate formation upon annealing.[35] For the Si 2p spectra, the Si 1+ state is seen to decrease, concurrent with an increase in the Si higher oxidation states upon HfO_2 ALD and the first annealing. The Si−Si bond is seen to decrease below the XPS detection limit after the second annealing at 500 °C, concurrent with an increase in the higher oxidation states (3+ and 4+), which may be related to Hf-silicate formation.[36] It is noted, however, that Hf-silicate formation from the reaction of Hf and SiO_2 or Si and HfO_2 generally occurs at higher annealing temperatures on Si substrates than those studied here for InP.[37−39] Moreover, silicide formation on Si after higher-temperature annealing has also been reported.[40] As such, we emphasize that the proposed Hf-silicate formation here is only speculation and requires further study.

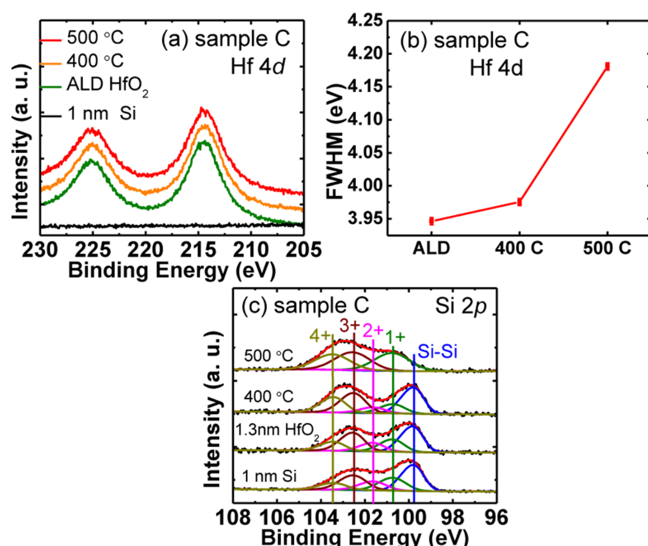

Figure 6. XPS from sample C upon Si deposition, after HfO_2 ALD, and after annealing at 400 and 500 °C under UHV: (a) Hf 4d; (b) FWHM of the Hf 4d spectra after HfO_2 ALD and following annealing; (c) Si 2p.

To conclusively establish the outermost surface atomic species present after the process steps, we employ LEIS. Figure 7 shows the ex situ LEIS spectra of (a) samples A and B using a He^+ source and (b) sample C using a Ne^+ source after UHV annealing at 500 °C. Both In feature is observed on the top surface of all of the samples studied, which is consistent with previous reports of In diffusion through ALD high-*k*/InP stacks upon annealing.[13,14] However, no Si or P is detectable from the LEIS spectra. This suggests that any silicates present are formed at the high-*k*/Si interface but not on the surface.

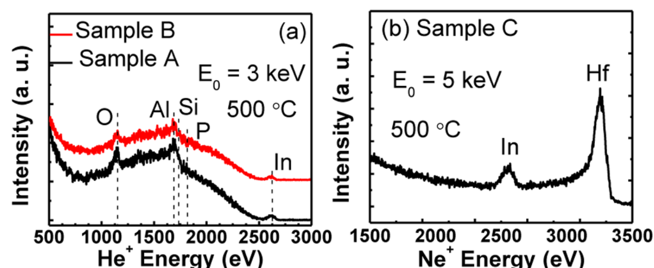

Figure 7. Ex situ LEIS results of (a) samples A and B using He^+ at 3000 eV and (b) sample C using Ne^+ at 5000 eV after annealing at 500 °C.

The schematic for the stack of sample B after annealing at 500 °C is shown in Figure 8. At the interface between the amorphous Si and the InP substrate, SiO_x is formed during the Si PECVD process. Al-silicate (Al−Si−O_x) may also form at the interface between Al_2O_3 and Si based upon the conditions employed here.[35,41] Diffusion of the In atoms on the stack surface likely occurs during the annealing process.[14]

For all samples, the In−In bonds are observed to persist throughout the Si IPL and high-*k* oxide layers, forming volatile

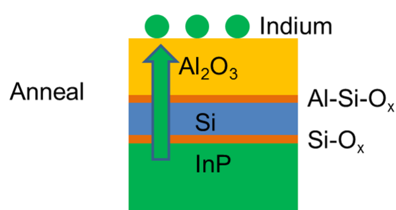

Figure 8. Schematic for the stack layers of sample B after annealing at 500 °C.

In_2O from the O-rich environment in high-*k* oxides,[42] and evaporate from the surface upon 400 °C annealing in UHV, resulting in a decrease in the concentration of In−In/Si bonding. For sample B, the In−In bond is seen to decrease upon the second annealing. However, for sample A, which has more In−In bond formation because of the reaction of Si with substantial concentrations of $InPO_x$, there is insufficient O available to form volatile In_2O after the second annealing. For sample C, the Hf-(silicate and oxide)/Si/InP interface is apparently not stable upon the second annealing. Therefore, among the structures investigated here, the Al-(silicate and oxide)/Si/InP stack of sample B is the most thermally stable. The In−In and P−P bonds generated during the Si PECVD process, possibly due to H radicals in the deposition environment, may induce gap states, as indicated from previous first-principle calculations, but are still under debate.[32,43]

CONCLUSIONS

In summary, the 1 nm Si IPL by PECVD can scavenge the In- and P-oxides significantly but not completely from the native oxide sample. The Si IPL can scavenge the In- and P-oxides completely from the acid-etched sample. The In−In/Si and P−Si/P bonds are formed by Si deposition. The formation of silicates of Al and Hf are considered during ALD and following annealing. Al-silicate formation with the Si/InP interface is more thermally stable. Hf-silicate formation is only speculated here, given the low temperatures employed. The optimum stack in this study was found to be Al_2O_3/Al-silicate/acid-etched InP, in terms of the minimized In−P-oxides and In−In/Si bond concentrations and highest thermal stability. In-diffusion through this Si IPL and high-k dielectric layer upon UHV annealing at 500 °C is detected on all samples. The minimization of In−P-oxides (below the XPS detection limit) from sample B is expected to minimize the interface trap density and requires further study.

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Notes

The authors declare no competing financial interest.

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REFERENCES

(1) Del Alamo, J. A. Nanometre-Scale Electronics with III−V compound semiconductors. *Nature* **2011**, *479*, 317−323.
(2) Frank, D. J. Power Constrained CMOS Scaling. *IBM J. Res. Dev.* **2002**, *46*, 235−244.
(3) Radosavljevic, M.; Dewey, G.; Fastenau, J. M.; Kavalieros, J.; Kotlyar, R.; Chu-Kung, B.; Liu, W. K.; Lubyshev, D.; Metz, M.; Millard, K.; Mukherjee, N.; Pan, L.; Pillarisetty, R.; Rachmady, W.; Shah, U.; Chau, R. Non-Planar, Multi-Gate InGaAs Quantum Well Field Effect Transistors with High-K Gate Dieletric and Ultra-Scaled Gate-to-Drain/Gate-to-Source Separation for Low Power Loigc Applications. *Int. Electron Devices Meet.* **2010**, 126−129.
(4) Lin, J.; Kim, T.-W.; Antoniadis, D. A.; Del Alamo, J. A. A Self-Aligned InGaAs Quantum-Well Metal−Oxide-Semiconductor Field-Effect Transistor Fabricated through a Lift-Off-Free Front-End Process. *Appl. Phys. Express* **2012**, *5*, 064002.
(5) Radosavljevic, M.; Chu-Kung, B.; Corcoran, S.; Dewey, G.; Hudait, M. K.; Fastenau, J. M.; Kavalieros, J.; Liu, W. K.; Lubyshev, D.; Metz, M.; Millard, K.; Mukherjee, N.; Rachmady, W.; Shah, U.; Chau, R. Advanced High-*K* Gate Dieletric for High-Performance Short-Channel InGaAs Quantum Well Field Effect Transistors on Si Substrate for Low Power Logic Applications. *Int. Electron Devices Meet.* **2009**, 319−322.
(6) Gu, J. J.; Neal, A. T.; Ye, P. D. Effect of $(NH_4)_2S$ Passivation on the Off-State Performance of 3-Dimensional InGaAs Metal−Oxide-Semiconductor Field-Effect Transistors. *Appl. Phys. Lett.* **2011**, *99*, 152113.
(7) Dewey, G.; Radosavljevic, M.; Pillarisetty, R.; Chau, R. Dual Layer Dielectrics for Non-Silicon Semiconductor Devices. U.S. Patent U.S. 8,227,833 B2, 2012.
(8) Cotal, H.; Fetzer, C.; Boisvert, J.; Kinsey, G.; King, R.; Heber, P.; Yoon, H.; Karam, N. III−V Multijuction Solar Cells for Concentrating Photovoltaics. *Energy Environ. Sci.* **2009**, *2*, 174−192.
(9) Brennan, B.; Dong, H.; Zhernokletov, D.; Kim, J.; Wallace, R. M. Surface and Interface Reaction Study of Half Cycle Atomic Layer Deposition Al_2O_3 on Chemically Treated InP Surfaces. *Appl. Phys. Express* **2011**, *4*, 125701.
(10) Dong, H.; Brennan, B.; Qin, X.; Zhernokletov, D. M.; Hinkle, C. L.; Kim, J.; Wallace, R. M. In Situ Study of Atomic Layer Deposition Al_2O_3 on InP. *Appl. Phys. Lett.* **2013**, *103*, 121604.
(11) Dong, H.; Brennan, B.; Zhernokletov, D.; Kim, J.; Hinkle, C. L.; Wallace, R. M. In situ Study of HfO_2 Atomic Layer Deposition on InP (100). *Appl. Phys. Lett.* **2013**, *102*, 171602.
(12) Galatage, R. V.; Dong, H.; Zhernokletov, D. M.; Brennan, B.; Hinkle, C. L. Electrical and Chemical Characteristics of Al_2O_3/InP Metal−Oxide-Semiconductor Capacitors. *Appl. Phys. Lett.* **2013**, *102*, 132903.
(13) Kang, Y. S.; Kim, C. Y.; Cho, M.-H.; Chung, K. B.; An, C.-H.; Kim, H.; Lee, H. J.; Kim, C. S.; Lee, T. G. Thickness dependence on Crystalline Structure and Interfacial Reactions in films on InP (001) grown by Atomic Layer Deposition. *Appl. Phys. Lett.* **2010**, *97*, 172108.
(14) Dong, H.; Cabrera, W.; Galatage, R. V.; Brennan, B.; Qin, X.; McDonnell, S.; Zhernokletov, D.; Hinkle, C. L.; Cho, K.; Chabal, Y. J.; Wallace, R. M. Indium Diffusion Through High-*K* Dielectrics in High-K/InP Stacks. *Appl. Phys. Lett.* **2013**, *103*, 061601.
(15) An, C.-H.; Byun, Y.-C.; Lee, M. S.; Kim, H. Thermal Stabilities of ALD-HfO_2 Films on HF- and $(NH_4)_2S$-Cleaned InP. *J. Electrochem. Soc.* **2011**, *158*, G242.
(16) McDonnell, S.; Dong, H.; Hawkins, J.; Brennan, B.; Milojevic, M.; Aguirre-Tostado, F.; Zhernokletov, D.; Hinkle, C.; Kim, J.; Wallace, R. Interfacial Oxide Re-Growth in Thin Film Metal Oxide III−V Semiconductor Systems. *Appl. Phys. Lett.* **2012**, *100*, 141606.
(17) Sun, Y.; Liu, Z.; Machuca, F.; Pianetta, P.; Spicer, W. E. Optimized Cleaning Method for Producing Device Quality InP (100) Surfaces. *J. Appl. Phys.* **2005**, *97*, 124902.

(18) Sun, Y.; Liu, Z.; Machuca, F.; Pianetta, P.; Spicer, W. E. Preparation of Clean InP (100) Surfaces Studies by Synchrotron Radiation Photoemission. *J. Vac. Sci. Technol. A* **2003**, *21*, 219−225.

(19) Wallace, R. M. In-Situ Studies of Interfacial Bonding of High-*k* Dielectrics for CMOS Beyond 22 nm. *ECS Trans.* **2008**, *16*, 255−271.

(20) Herrera-Gomez, A.; Hedegus, A.; Meisssner, P. L. Chemical Depth Profile of Ultrathin Nitrided SiO_2 Films. *Appl. Phys. Lett.* **2002**, *81*, 1014−1016.

(21) Brongersma, H.; Draxler, M.; Deridder, M.; Bauer, P. Surface Composition Analysis by Low-Energy Scattering. *Surf. Sci. Rep.* **2007**, *62*, 63−109.

(22) Kuwahara, T.; Ito, H.; Kawaguchi, K.; Higuchi, Y.; Ozawa, N.; Kubo, M. Different Crystal Growth Mechanisms of Si (001)-(2×1): H during Plasma-Enhanced Chemical Vapor Deposition of SiH_3 and SiH_2 Radicals: Tight-Binding Quantum Chemical Molecular Dynamics Simulaitons. *J. Phys. Chem. C* **2013**, *117*, 15602−15614.

(23) Tanenbaum, D.; Laracuente, A.; Gallagher, A. Surface Roughening during Plasma-Enhanced Chemical-Vapor Deposition of Hydrogenated Amorphous Silicon on Crystal Silicon Substrates. *Phys. Rev. B* **1997**, *56*, 4243−4250.

(24) Gao, K. Y.; Speck, F.; Emtsev, K.; Seyller, T.; Ley, L.; Oswald, M.; Hansch, W. Interface of Atomic Layer Deposited Al_2O_3 on H-Terminated Silicon. *Phys. Status Solidi* **2006**, *203*, 2194−2199.

(25) Frank, M. M.; Chabal, Y. J.; Wilk, G. D. Nucleation and Interface Formation Mechanisms in Atomic Layer Deposition of Gate Oxides. *Appl. Phys. Lett.* **2003**, *82*, 4758−4760.

(26) Hollinger, G.; Bergignat, E.; Joseph, J. On the Nature of Oxides on InP Surfaces. *J. Vac. Sci. Technol. A* **1985**, *3*, 2082−2088.

(27) Faur, M.; Faur, M.; Jayne, D. T.; Goradia, M.; Goradia, C. XPS Investigation of Anodic Oxides Grown on p-type InP. *Surf. Interface Anal.* **1990**, *15*, 641−650.

(28) Himpsel, F. J.; McFeely, F. R.; Taleb-Ibrahimi, A.; Yarmoff, J. A.; Hollinger, G. Microscopic Structure of the SiO_2/Si Interface. *Phys. Rev. B* **1988**, *38*, 6084−6096.

(29) Wagner, C. D.; Passoja, D. E.; Hillery, H. F.; Kinisky, T. G.; Six, H. A.; Jansen, W. T.; Taylor, J. A. Auger and Photoelectron Line Energy Relationships in Aluminum-Oxygen and Silicon-Oxygen Compounds. *J. Vac. Sci. Technol.* **1982**, *21*, 933−944.

(30) Koo, J.; Kim, S.; Jeon, S.; Jeon, H.; Kim, Y. Characteristics of Al_2O_3 Thin Films Deposited Using Dimethylaluminum Isopropoxide and Trimethylaluminum Precursors by the Plasma-Enhanced Atomic-Layer Deposition Method. *J. Korean Phys. Soc.* **2006**, *48*, 131−136.

(31) Zhu, Z.; Jiang, T.; Li, G.; Guo, Y.; Yang, Y. *Interaction Studies—Solids, Liquids and Gases*; Intech: Winchester, U.K., 2011.

(32) Komsa, H.; Pasquarello, A. Identification of Defect Levels at As/Oxide Interfaces Through Hybrid Functionals. *Microelectron. Eng.* **2011**, *88*, 1436−1439.

(33) Casey, P.; Hughes, G. Interfacial Analysis of InP Surface Preparation Using Atomic Hydrogen Cleaning and Si Interfacial Control Layers Prior to MgO Deposition. *Appl. Surf. Sci.* **2010**, *256*, 7530−7534.

(34) Klein, T. M.; Niu, D.; Epling, W. S.; Li, W.; Maher, D. M.; Hobbes, C.; Hedge, R.; Baumvol, I. J. R.; Parsons, G. N. Evidence of Aluminum Silicate Formation during Chemical Vapor Deposition of Amorphous Al_2O_3 Thin Films on Si (100). *Appl. Phys. Lett.* **1999**, *75*, 4001−4003.

(35) Wilk, G. D.; Wallace, R. M.; Anthony, J. M. Hafnium and Zirconium Silicates for Advanced Gate Dielectrics. *J. Appl. Phys.* **2000**, *87*, 484−492.

(36) Schmeisser, D.; Zheng, F.; Himpsel, F. J.; Engelmann, H. J. Silicate Formation at the Interface of High-*k* Dielectrics and Si (001) Surfaces. *Mater. Res. Soc. Symp. Proc.* **2006**, *917*, 0917−E10-02.

(37) Lee, J.-H.; Ichikawa, M. Analysis of Interfacial Silicates and Silicides Formed by Annealing Ultrathin: Hf on SiO_2: Effect of Hf/SiO_2 Thickness Ratio. *J. Appl. Phys.* **2002**, *92*, 1929−1935.

(38) Lin, Y.-S.; Puthenkovilakam, R.; Chang, J. P. Dielectric Property and Thermal Stability of HfO_2 on Silicon. *Appl. Phys. Lett.* **2002**, *81*, 2041−2043.

(39) Deshpande, A.; Inman, R.; Jurisch, G.; Takoudis, C.G. Annealing Behavior of Atomic Layer Deposited Hafnium Oxide on Silicon: Changes at the Interface. *J. Appl. Phys.* **2006**, *99*, 094102.

(40) Lebedinskii, Y. Y.; Zenkevich, A.; Gusev, E.P.; Gribelyuk, M. In Situ Investigation of Growth and Thermal Stability of Ultrathin Si Layers on the HfO_2/Si (100) High-*k* Dielectric System. *Appl. Phys. Lett.* **2005**, *86*, 191904.

(41) Hinkle, C. L.; Milojevic, M.; Vogel, E. M.; Wallace, R. M. Surface Passivation and Implications on High Mobility Channel Performance. *Microelectron. Eng.* **2009**, *86*, 1544−1549.

(42) Valderraman, J.; Jacob, K. T. Vapor Pressure and Dissociation Energy of (In_2O). *Thermochim. Acta* **1977**, *21*, 215−224.

(43) Lin, L.; Robertson, J. Defect States at III−V Semiconductor Oxide Interfaces. *Appl. Phys. Lett.* **2011**, *98*, 082903.